What is claimed is:

1. A pixel layout for a line image sensor, wherein the improvement comprises, said line image sensor is formed by a plurality of pixels being arranged in two pixel rows to raise the resolution, and said two pixel rows are interlacing by pixels in accordance.

2. The pixel layout for a line image sensor of claim 1, wherein said two pixel rows are arranged in parallel.

3. The pixel layout for a line image sensor of claim 1, wherein said two pixel rows are arranged in parallel and each pixel in one row is alternating with other two pixels in another row.

4. The pixel layout for a line image sensor of claim 1, wherein said line image sensor is fabricated by the technology of Charge-Couple Device (CCD).

5. The pixel layout for a line image sensor of claim 1, wherein said line image sensor is fabricated by the technology of Complementary Metal-Oxide Semiconductor (CMOS).

6. A pixel layout for a line image sensor, wherein the improvement comprises, said line image sensor is formed by a plurality of pixels being arranged in more than even pixel rows to raise the resolution, and pixels of said more than even pixel rows are interlacing with each other.

7. The pixel layout for a line image sensor of claim 6,

wherein said more than even pixel rows are arranged in parallel.

8. The pixel layout for a line image sensor of claim 6, wherein said more than even pixel rows are arranged in parallel and each pixel of one row is alternating with other two pixels of adjacent row.

9. The pixel layout for a line image sensor of claim 6, wherein said line image sensor is fabricated by the technology of Charge-Couple Device (CCD).

10. The pixel layout for a line image sensor of claim 6, wherein said line image sensor is fabricated by the technology of Complementary Metal-Oxide Semiconductor (CMOS).

11. A pixel layout for a line image sensor, wherein the improvement comprises, the line image sensor is formed by a plurality of pixels being arranged in a plurality parallel rows to raise the resolution, and said more than two parallel rows are arranged closely, which pixels of said plurality parallel rows are interlacing with each other in accordance.

12. The pixel layout for a line image sensor of claim 11, wherein said line image sensor is fabricated by the technology of Charge-Couple Device (CCD).

13. The pixel layout for a line image sensor of claim 11, wherein said line image sensor is fabricated by the technology of Complementary Metal-Oxide Semiconductor

(CMOS).